

LSI LOGIC

Rapid
CHIP

Processor Cores
"Putting Silicon IP To Work"

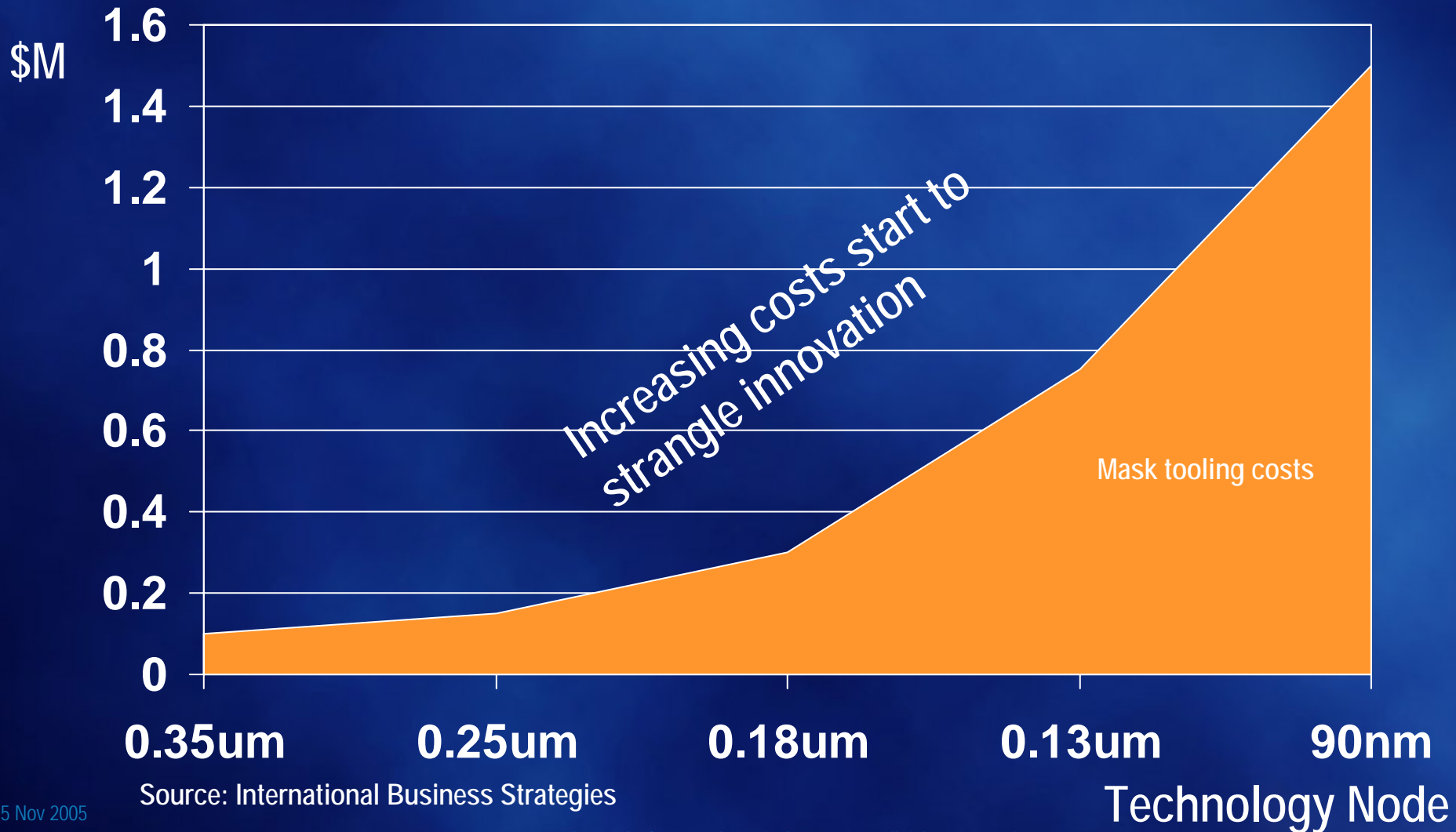
Structured ASICs and their use in Embedded IP SOC Designs

Mon 5th Dec 14:40-15:10 (30min)

Tim Daniels

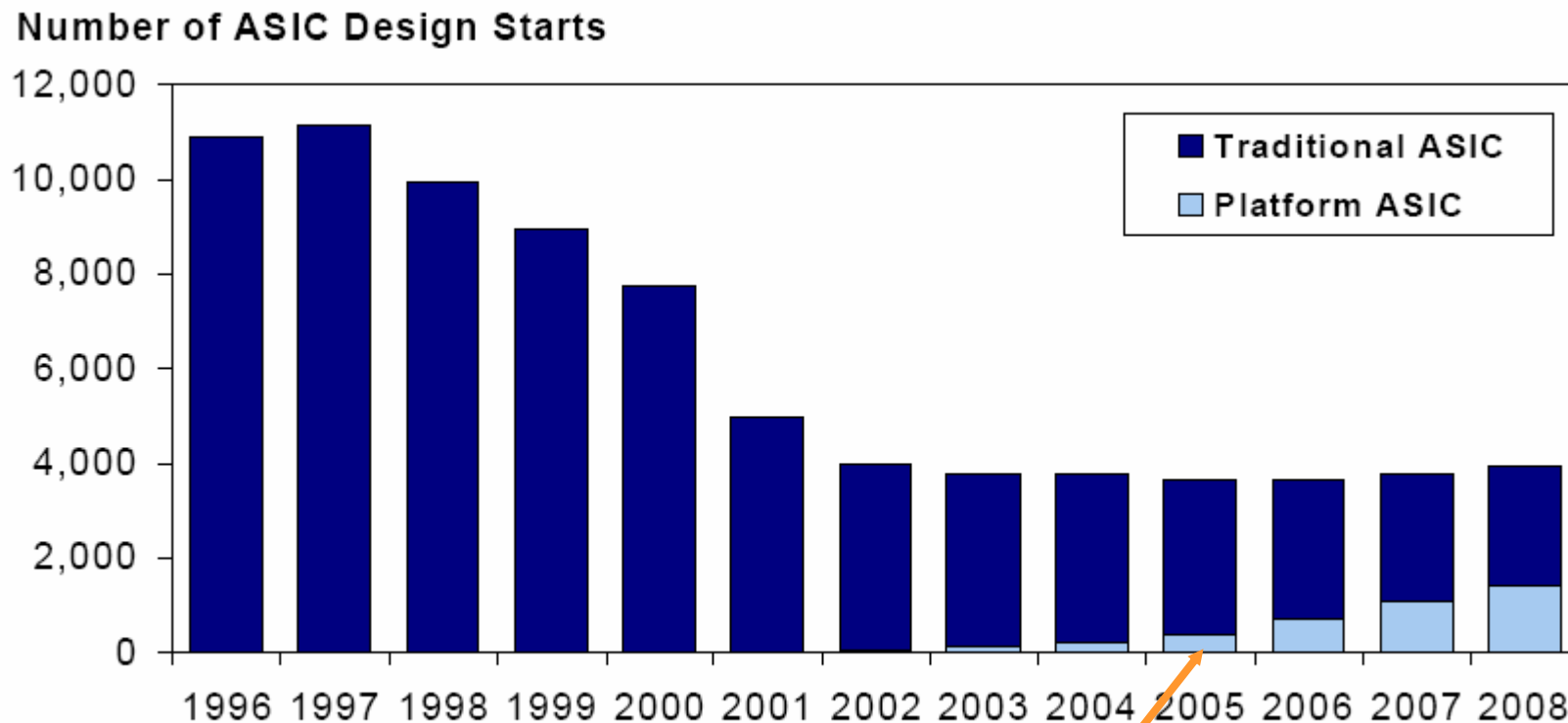
25 Nov 05

Cell-Based ASIC Mask Tooling Costs



Source: International Business Strategies

Changing ASIC Landscape



Source: Gartner Dataquest (June 2005)

Platform ASIC re-enables innovation

Combining the benefits of:

Cell-Based ASICs

- High Performance (3x of FPGA)
- Low Power (10th of FPGA)
- High Density (5x of FPGA)
- Product Differentiation
- Proven High Value Intellectual Property
- + Lower Cost (\$50-150K)

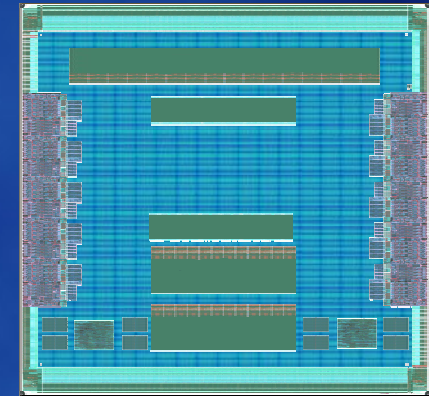


FPGAs

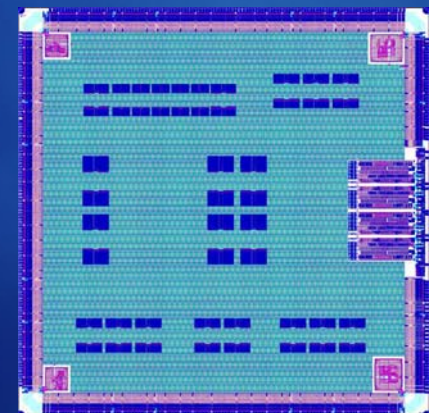
- Easy to Use Design Tools
- Configurability
- Short Time to Execute

RapidChip™ Platform ASIC

- Configurable Platform
 - Families of pre-manufactured slices
 - Customized with 4 layers of metal
 - Sea of transistors for user-configurable logic
 - Flexible approach to IP:
 - Diffused SerDes IP
 - “On-demand” for majority of cores
 - Landing Zones – pre-defined locations for critical cores
 - Soft – anything else

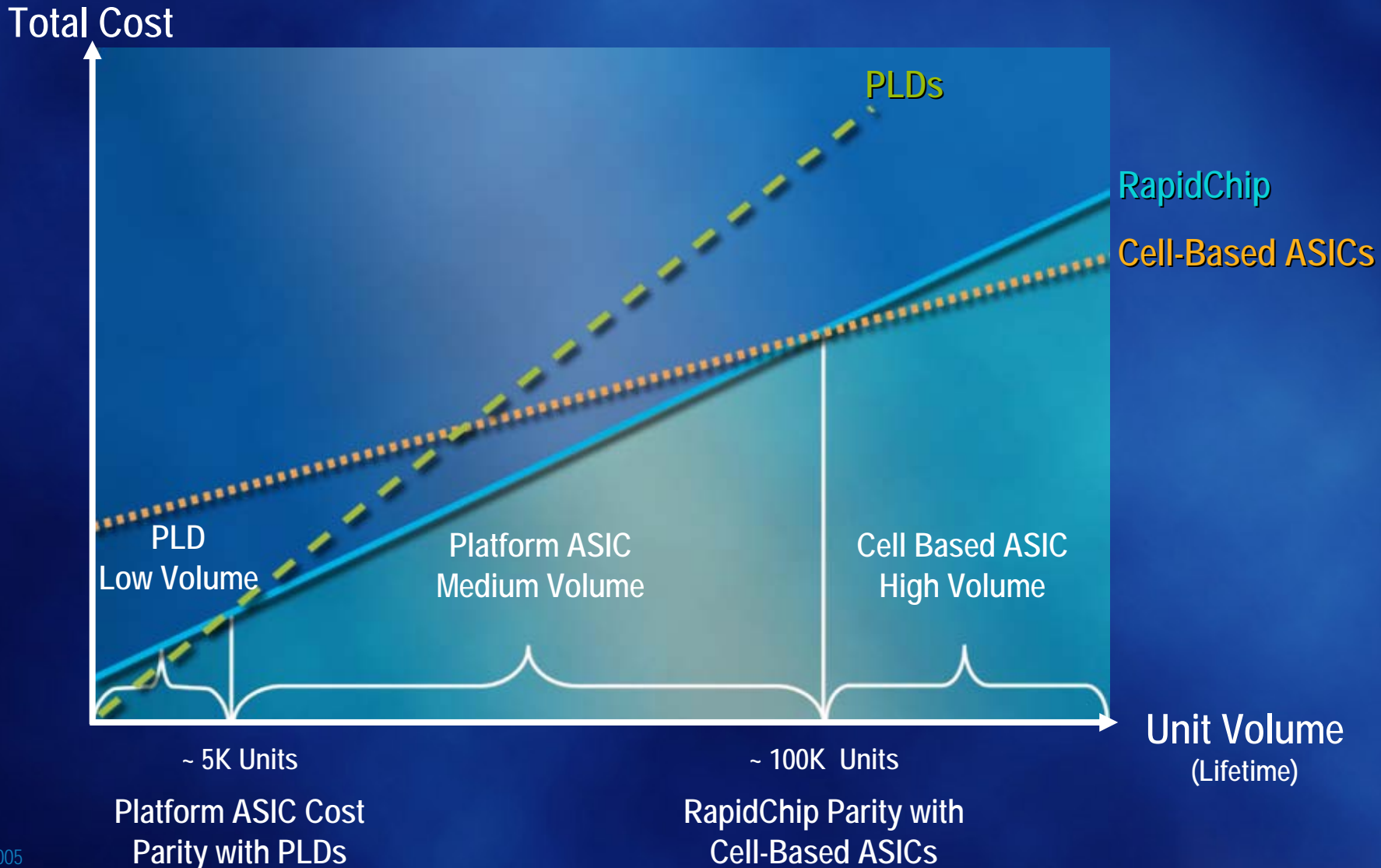


Xtreme2



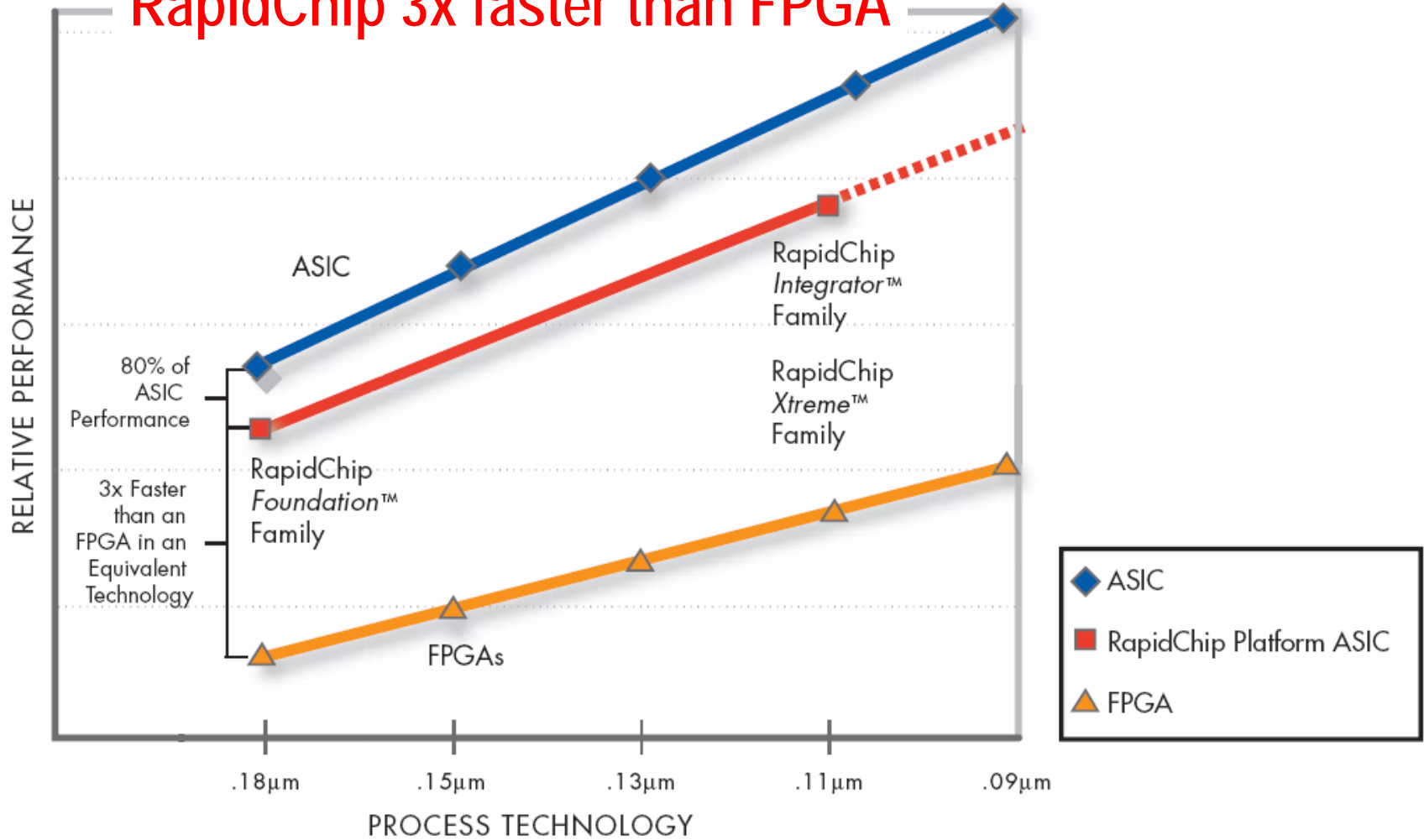
IntegratorQS

Customer Product Unit Volume



Relative Performance

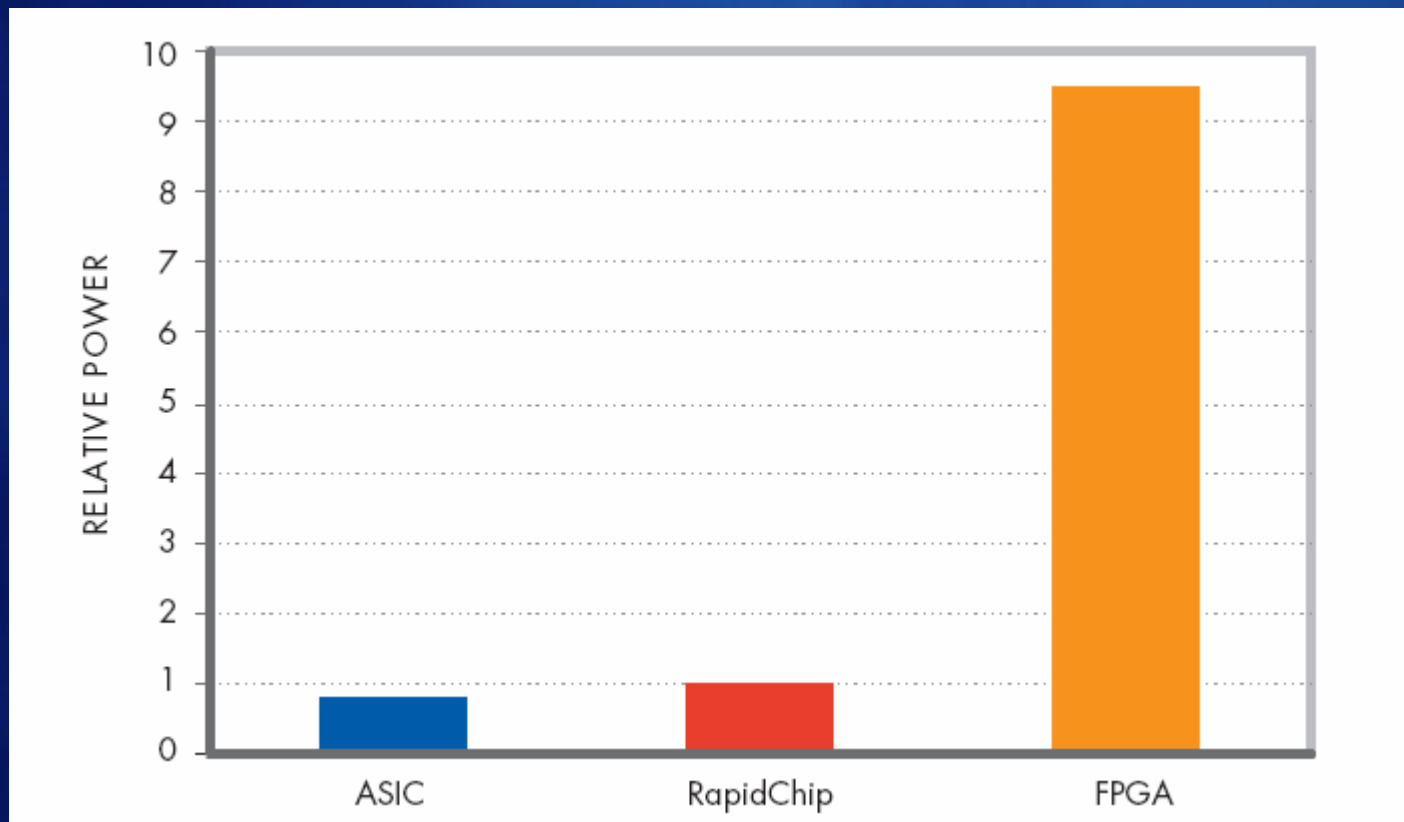
RapidChip 3x faster than FPGA



Source: RC Vs FPGA White Paper, LSI Logic

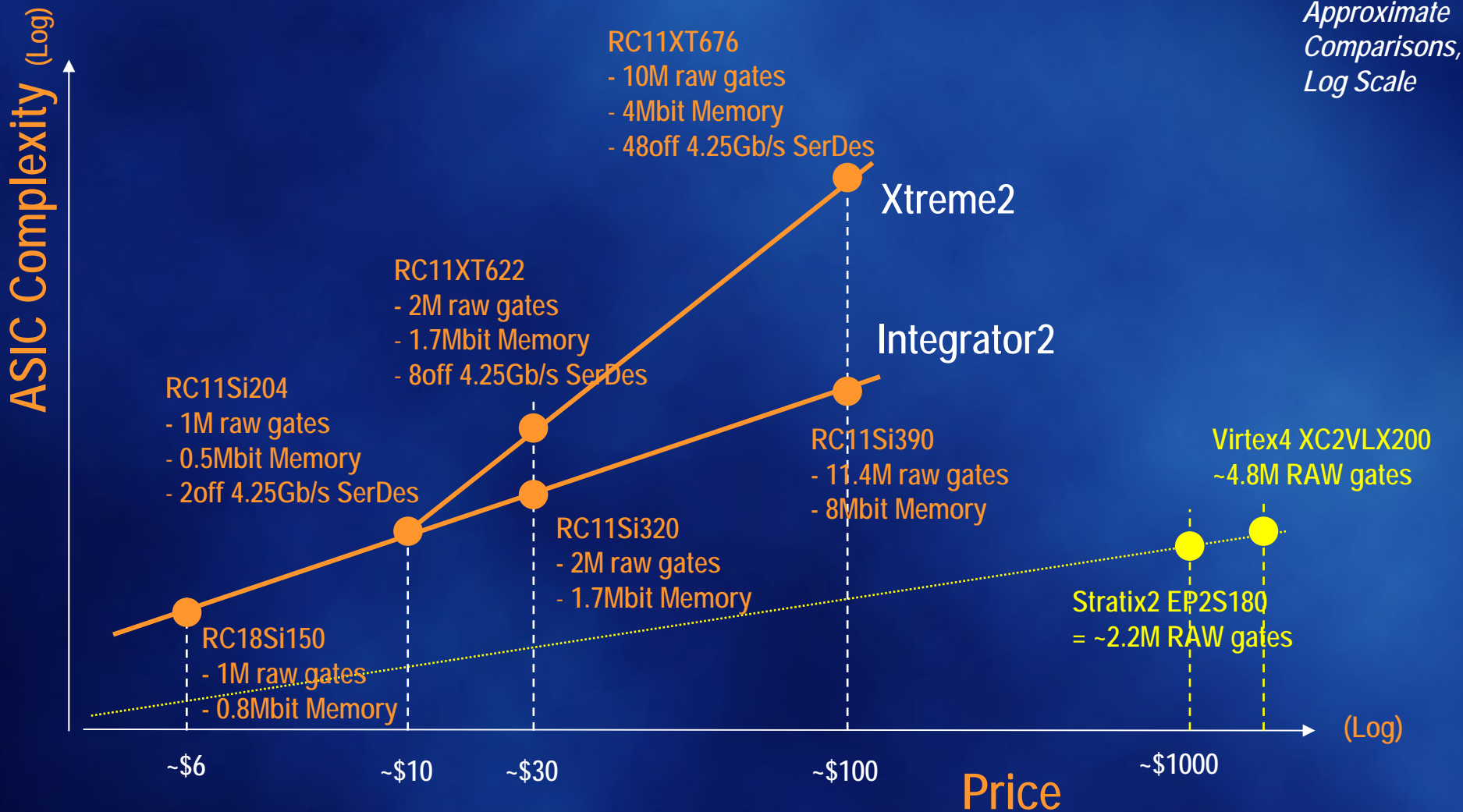
Relative Power

RapidChip 10x less power than FPGA

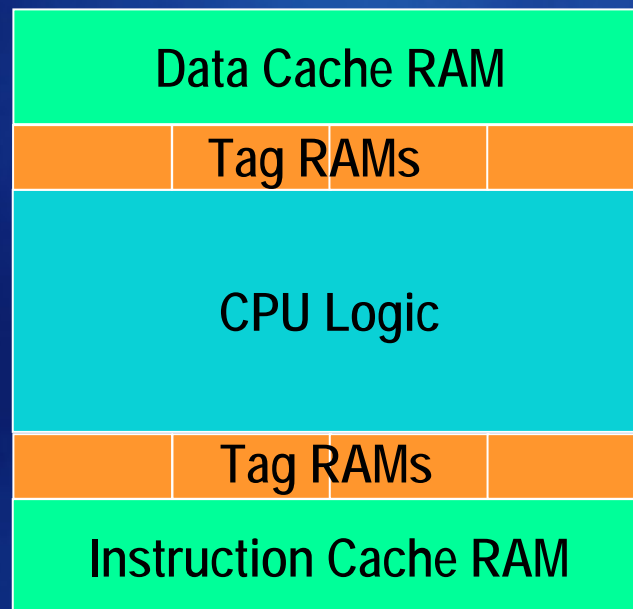


Source: RC Vs FPGA White Paper, LSI Logic

Price Vs Complexity

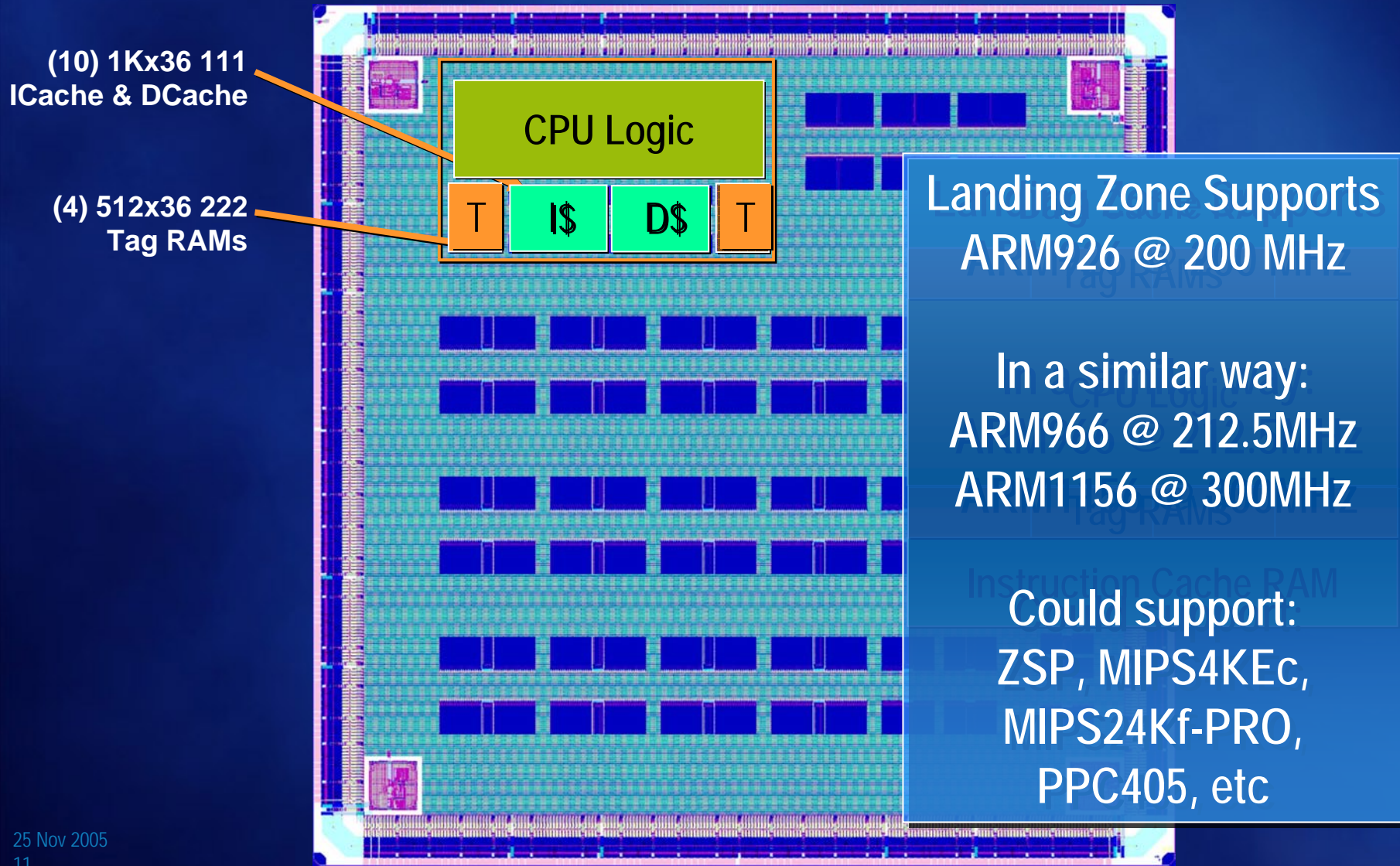


Example Critical IP - Processor



- The physical relationship of the memories and CPU Logic are critical factors in processor performance and architecture

Landing Zone™ on RC11Si240 Slice



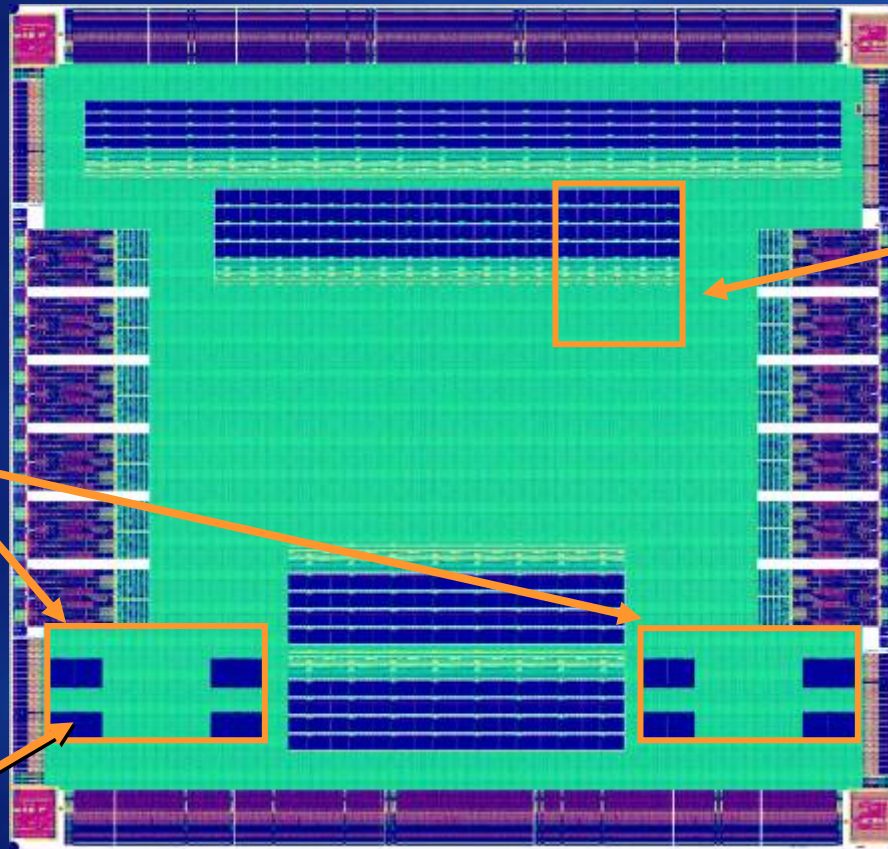
Landing Zone Supports
ARM926 @ 200 MHz

In a similar way:
ARM966 @ 212.5MHz
ARM1156 @ 300MHz

Could support:
ZSP, MIPS4KEc,
MIPS24Kf-PRO,
PPC405, etc

Multi-Processor Designs

- Becoming more common...



Further "Multi-Site"
Landing Zone™
available:
ARM926, ARM966,
ARM1156

Could support: MIPS
etc if demand requires

2off - "Fixed"
Landing Zone™ for
ARM966 or ARM1156

(4) 4Kx36 111
I&D TCM RAMs

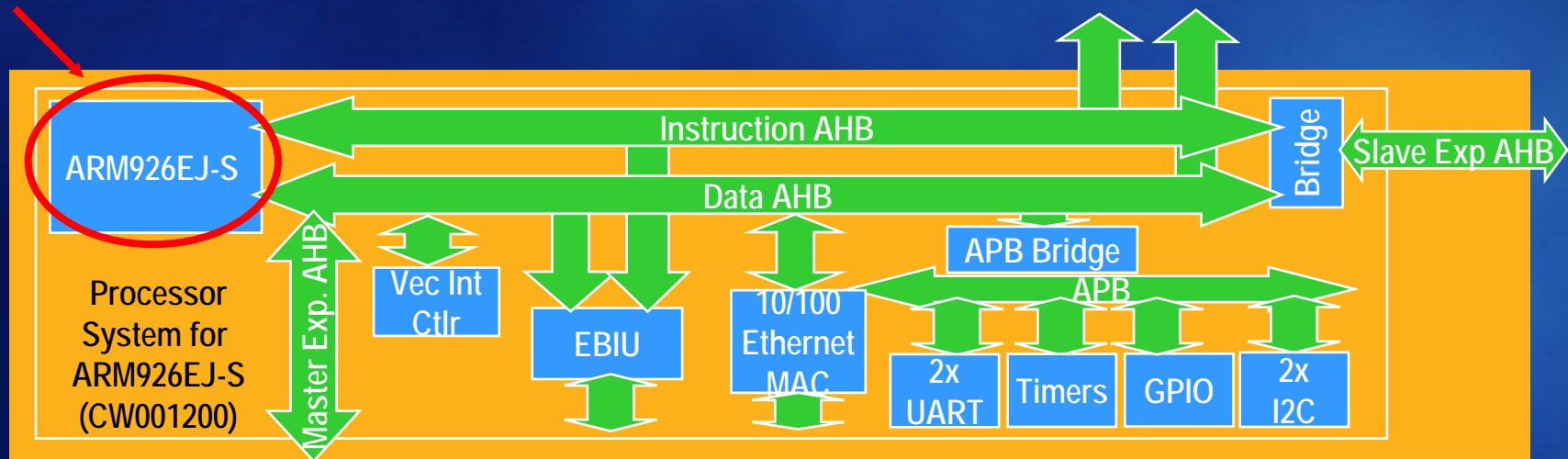
Slice: RC11XT676

Complete Sub-Systems

But the CPU (& memory) is not enough....

- Ready to use “system”, easily expandable
- Complete with verification environment, user guide etc

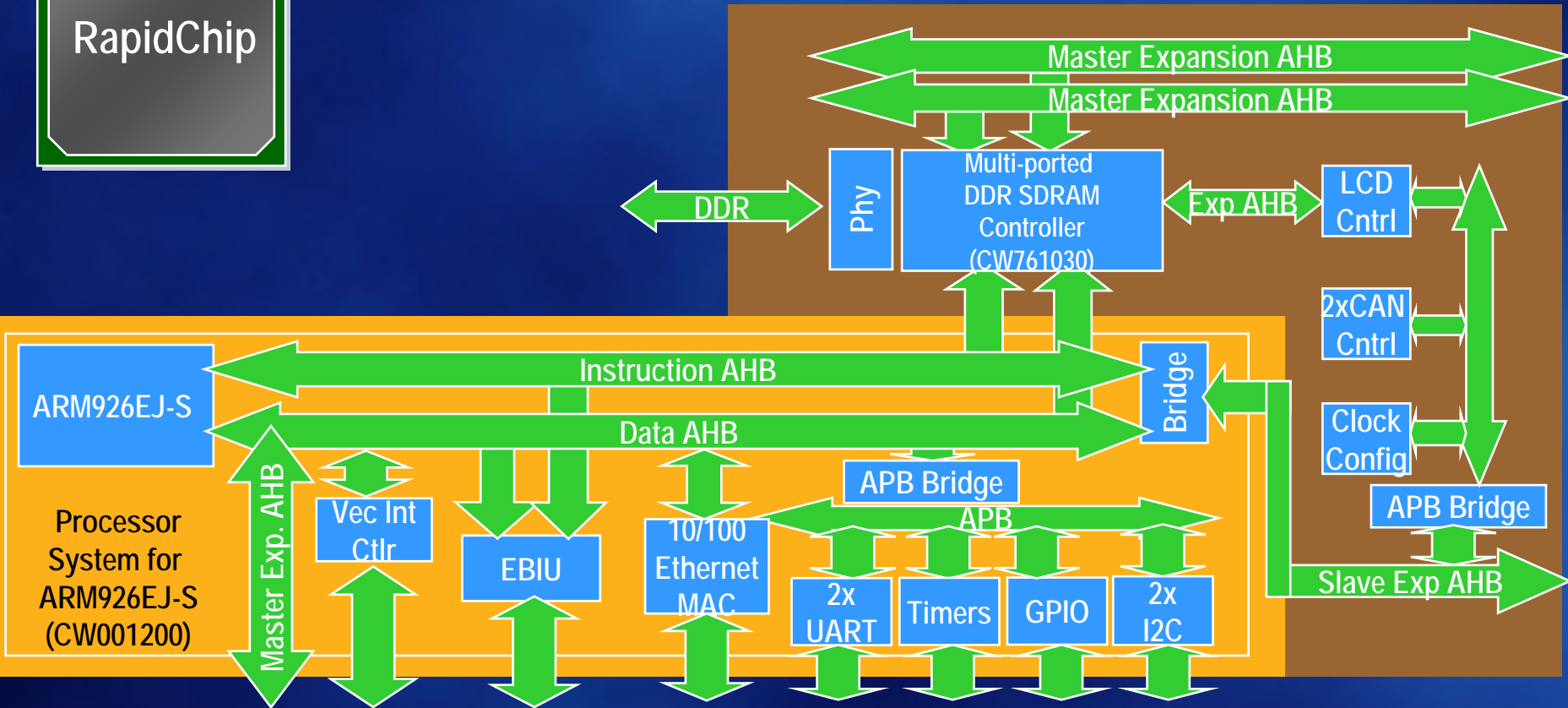
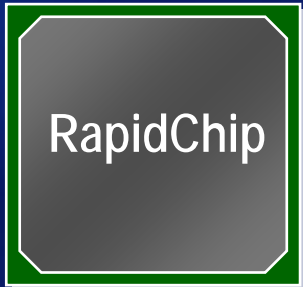
Landing Zone



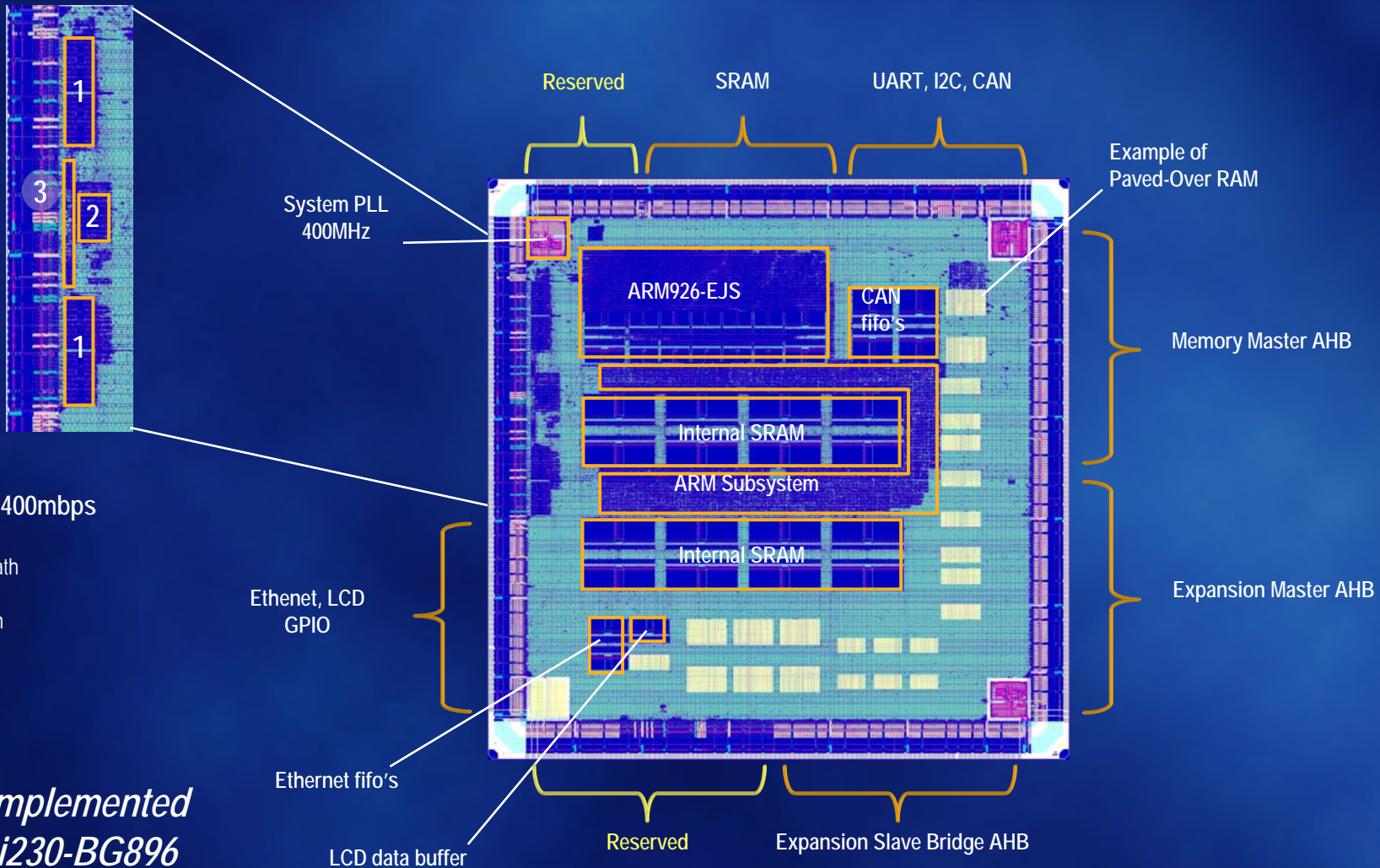
Reference Design for MIPS also available

A Simple SoC Design.....

ARM926EJ-S Eval Chip



Anatomy of The ARM926EJ-S Eval Chip



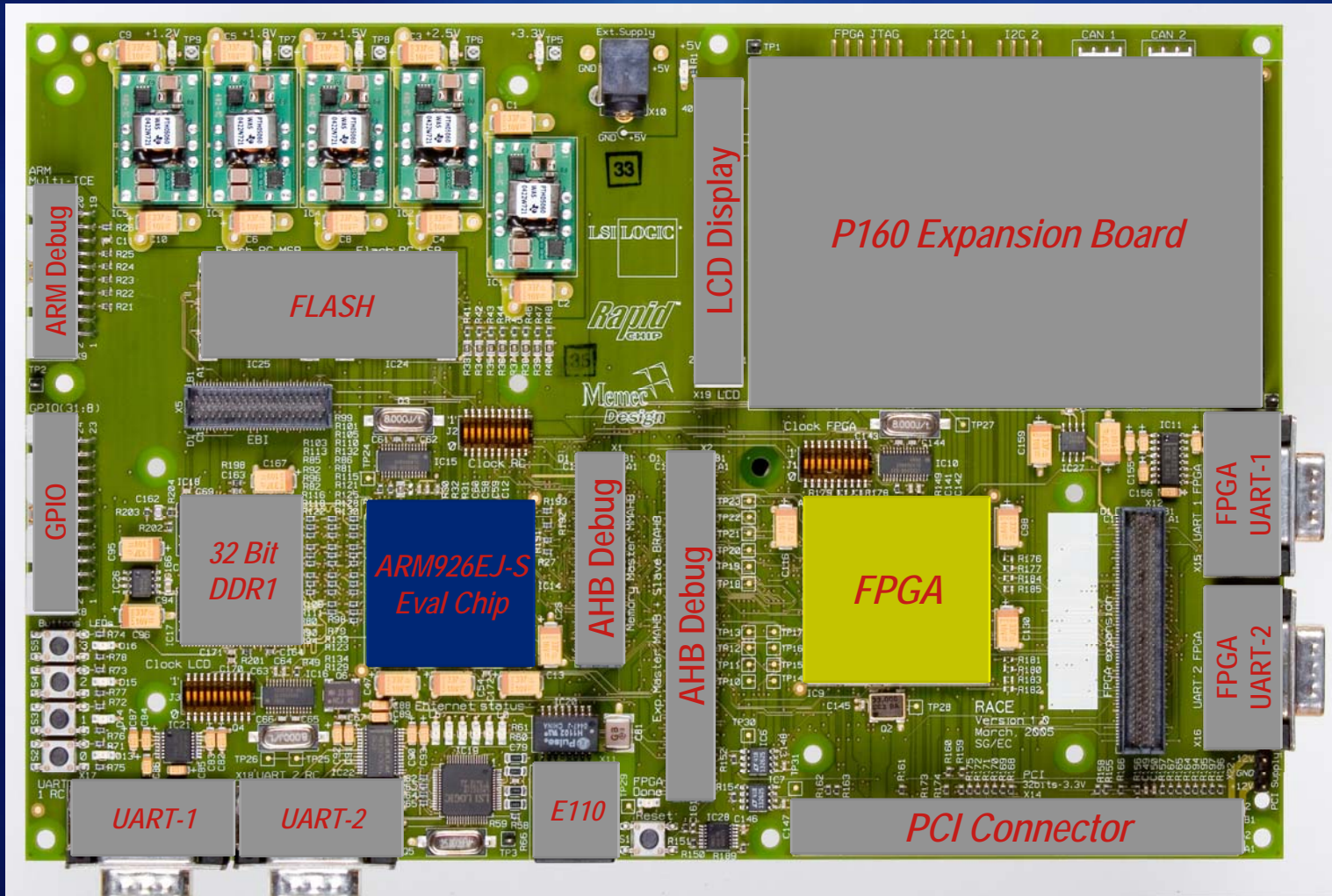
DDR interface
32Bit 200MHz / 400mbps

- 1) DDR PHY datapath
- 2) Master DLL
- 3) Address datapath

*Instance Implemented
on RC11Si230-BG896*

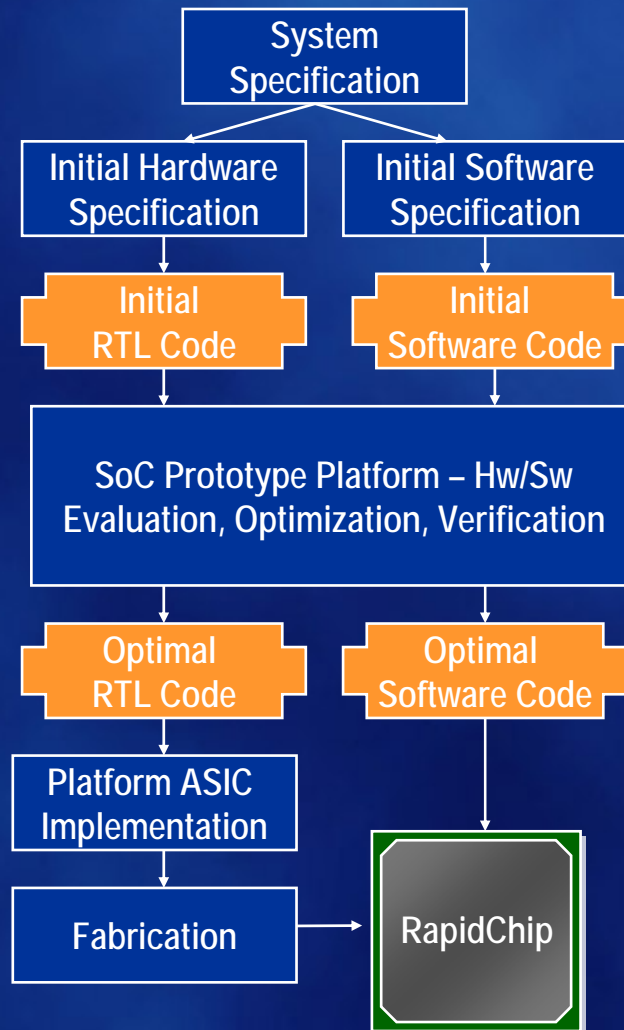
ARM926EJ-S SoC Prototyping Platform

Board Layout - Top Side



Board Dimensions: 240mm x 160mm
9.4" x 6.3"

Typical Design flow

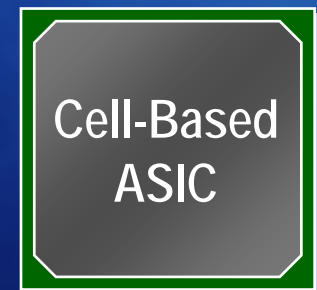
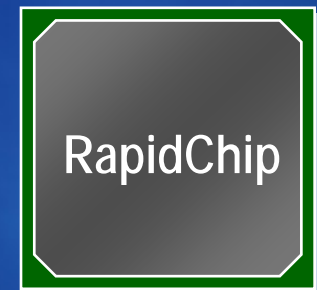


SoC Prototyping Usage Model

- Eval Board – Early Prototyping
 - Hardware/Software debug
 - Lab model

- Platform ASIC – SoC Market vehicle
 - Cost effective
 - High performance, low risk

- Cell-Based ASIC
 - Easy Migration to our Cell-Based offering, if volumes make sense
 - Ultimate low cost for high volume products



IP Partners – Key to Platform Design



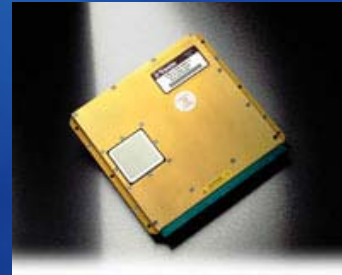
- We qualify both the IP Partner and their IP block
 - VSIA “QIP” checklist – pre-screen
- IP synthesised & placed onto a RapidChip slice
 - Finds any integration issues
- Partner IP extends our trusted CoreWare IP catalogue
 - Denali Memory Controller, ARM Primecells, GDA PCI-Express I/F, PLDA PCI I/F etc etc

RapidChip Customer Example

-- Aircraft Navigation GPS



- Early 6 Chip prototype
- 1 RapidChip -- RC11Si231
 - ARM926 200MHz
 - 3.5M gates
 - 2.6MBit memory
- Force524 GPS has 24 channels
 - With 24 correlators per channel
 - Plus large correlator array
- Benefit
 - 50% less development time
 - 75% less NRE comparing to ASIC
 - Lower risk, higher performance



"Our design schedule was of utmost concern, and that was one reason we chose the RapidChip Platform ASIC so we could achieve quick time to market."

Ron Smith

**General Manager. Military and
Advanced Systems, Trimble**

RapidChip Customer Example

-- IP Wireless – Broadband Wireless



- Secure mobile broadband – WW markets
- Initially prototypes in 3xFPGA
- Migrated to RapidChip Platform ASIC
- Reasons to go to Platform ASIC
 - IP Protection (No code in SRAM)
 - Power Saving (6W->1W)
 - Cost (85% saving overall)
 - Small form factor (smaller PCB)



NodeB Base Station

Summary

- Platform ASIC
 - SoC ASIC Design for 90/65nm
 - High Performance & Low Power
 - Quick to market & affordable

- SoC Prototyping Platform
 - Complete CPU sub-system solves integration issues
 - Enables system architecture optimization
 - Allows Hw/Sw debug, lowering risk & timescale

- Partner IP
 - Essential for today's complex SoC designs